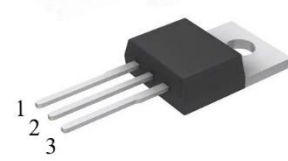




# P3M06060T3 SiC MOS N-Channel Enhancement Mode

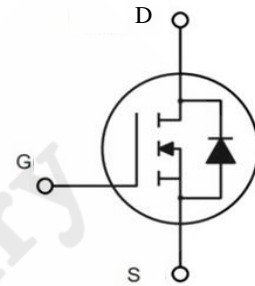
$V_{RRM}$	=	650	V
$I_D$	=	46	A
$I_D(100^\circ\text{C})$	=	33	A
$R_{DS(on)}$	=	60	mΩ

## SiC MOS P3M06060T3 N-Channel Enhancement Mode



### Features

- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small  $Q_{gd}$
- 100% UIS tested



### Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

TO-220-3

Gate	1
Drain	2
Source	3

### Applications

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies



### Order Information

Part Number	Package	Marking
P3M06060T3	TO-220-3	P3M06060T3



## Contents

Features.....	1
Benefits.....	1
Applications.....	1
Order Information .....	1
<b>Contents.....</b>	<b>2</b>
1. Maximum Ratings.....	3
2. Electrical Characteristics .....	4
3. Reverse Diode Characteristics.....	6
4. Thermal Characteristics.....	6
5. Typical Performance .....	7
6. Definitions .....	11
7. Package Outlines.....	12

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## 1. Maximum Ratings

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	$V_{DSmax}$	650	V	$V_{GS} = -3V$ $I_D = 100\mu A$
Gate - Source Voltage (dynamic)	$V_{GSmax}$	-8 / +20	V	AC ( $f > 1\text{ Hz}$ )
Gate - Source Voltage (static)	$V_{GSop}$	-3 / +15	V	Static
Continuous Drain Current	$I_D$	46	A	$V_{GS} = 15V$ $T_C = 25^\circ\text{C}$
		33		$V_{GS} = 15V$ $T_C = 100^\circ\text{C}$
Power Dissipation	$P_D$	170	W	
Operating Junction	$T_J$	-55 To +175	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$	-55 To +175	$^\circ\text{C}$	
Solder Temperature	$T_L$	260	$^\circ\text{C}$	
Mounting Torque	$M_d$	1 8.8	Nm lbf-in	M3 or 6-32 screw



## 2. Electrical Characteristics

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	/	/	V	$V_{GS} = -3\text{V}$ $I_D = 100\mu\text{A}$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.2	/	V	(tested after 30ms pulse at $V_{GS} = 15\text{V}$ ) $V_{DS} = V_{GS}$ $I_D = 20\text{mA}$ $T_J = 25^\circ\text{C}$
		/	1.65	/	V	$V_{DS} = V_{GS}$ $I_D = 20\text{mA}$ $T_J = 175^\circ\text{C}$
Reverse Bias Drain Current	$I_{DSS}$	/	0.5	10	$\mu\text{A}$	$V_{GS} = -3\text{V}$ $V_{DS} = 650\text{V}$
Gate-Source Leakage Current	$I_{GSS}$	/	20	250	nA	$V_{GS} = 15\text{V}$ $V_{DS} = 0\text{V}$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	60	79	m $\Omega$	$V_{GS} = 15\text{V}$ $I_D = 20\text{A}$
		/	52	/	m $\Omega$	$V_{GS} = 18\text{V}$ $I_D = 20\text{A}$
Trans conductance	$g_{fs}$	/	12	/	S	$V_{DS} = 20\text{V}$ $I_{DS} = 20\text{A}$ $T_J = 25^\circ\text{C}$
		/	11	/	S	$V_{DS} = 20\text{V}$ $I_{DS} = 20\text{A}$ $T_J = 175^\circ\text{C}$



# P3M06060T3 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Input Capacitance	$C_{iss}$	/	1911	/	pF	$V_{GS} = 0V$ $V_{DS} = 400V$ $f = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	$C_{oss}$	/	162	/	pF	
Reverse Transfer Capacitance	$C_{rss}$	/	15.3	/	pF	
Coss Stored Energy	$E_{oss}$	/	15	/	$\mu$	
Turn-on Energy	$E_{on}$	/	172.8	/	$\mu$	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Turn-off Energy	$E_{off}$	/	29.2	/		
Turn-On Delay Time	$t_{d(on)}$	/	15.5	/	nS	$V_{DS} = 400V$ $V_{GS} = -3/15V$ $I_D = 20A$ $R_G = 1\Omega$
Rise Time	$t_r$	/	27.2	/		
Turn-Off Delay Time	$t_{d(off)}$	/	24.3	/		
Fall Time	$t_f$	/	15.5	/		
Internal Gate Resistance	$R_{G(int)}$	/	1.06	/	$\Omega$	$f = 1MHz$ $V_{AC} = 25mV$
Gate to Source Charge	$Q_{gs}$	/	17.5	/	nC	$V_{DS} = 400V$ $I_{DS} = 20A$ $V_{GS} = -3 \text{ to } 15V$ $I_G = 50mA$
Gate to Drain Charge	$Q_{gd}$	/	15.3	/		
Total Gate Charge	$Q_g$	/	53.1	/		

### 3. Reverse Diode Characteristics

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	$V_{SD}$	4.8	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 25^\circ\text{C}$
		4.3	/	V	$V_{GS} = -3\text{V}$ $I_{SD} = 10\text{A}$ $T_J = 175^\circ\text{C}$
Continuous Diode Forward Current	$I_S$	27	/	A	$V_{GS} = -3\text{V}$
Reverse Recover Time	$t_{rr}$	29.6	/	nS	$V_{GS} = -3\text{V}$ $I_{SD} = 20\text{A}$ $V_R = 400\text{V}$ $d_{if}/d_t = 3100\text{A}/\mu\text{s}$ $T_J = 25^\circ\text{C}$
Reverse Recovery Charge	$Q_{rr}$	273	/	nC	
Peak Reverse Recovery Current	$I_{rrm}$	15.6	/	A	

### 4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.88	$^\circ\text{C}/\text{W}$

## 5. Typical Performance

At  $T_J = 25^\circ\text{C}$ , unless specified otherwise

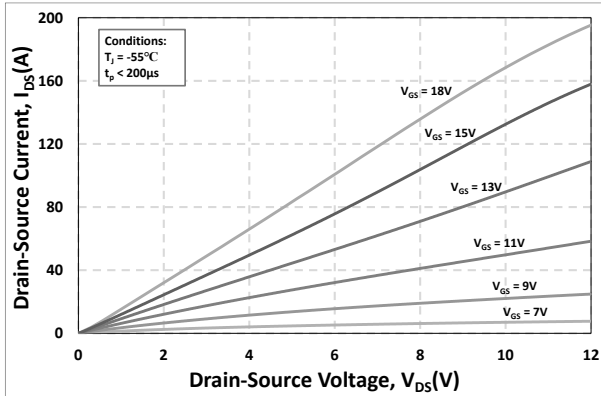


Figure 1. Output Characteristics  $T_J = -55^\circ\text{C}$

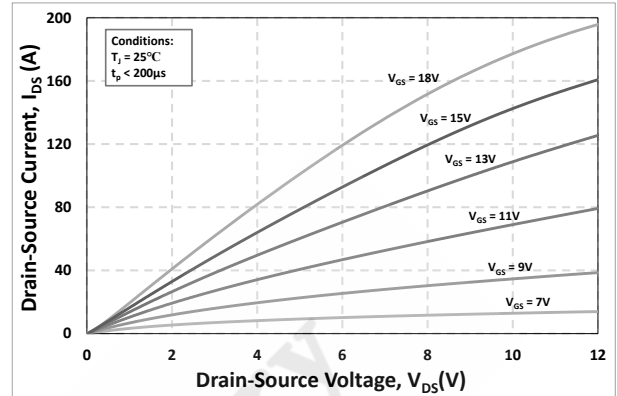


Figure 2. Output Characteristics  $T_J = 25^\circ\text{C}$

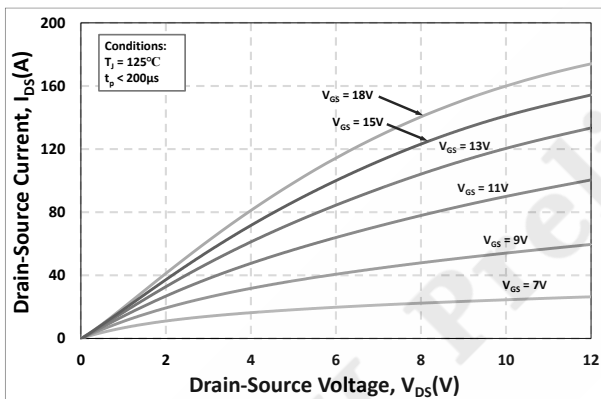


Figure 3. Output Characteristics  $T_J = 125^\circ\text{C}$

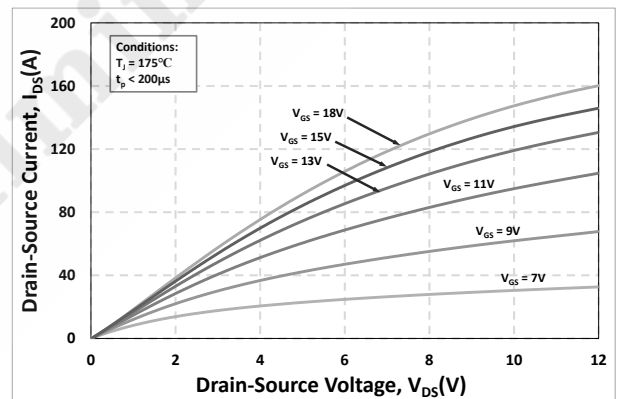


Figure 4. Output Characteristics  $T_J = 175^\circ\text{C}$

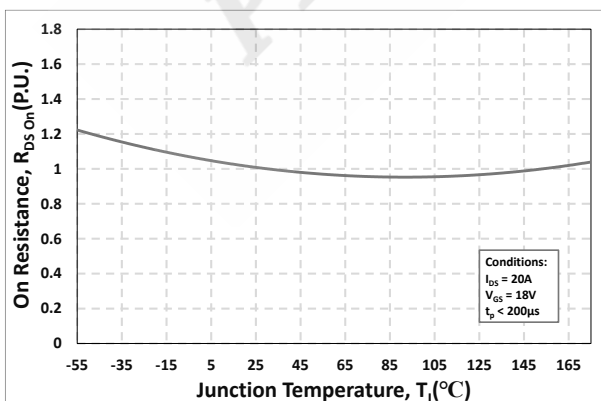


Figure 5. Normalized On-Resistance vs. Temperature

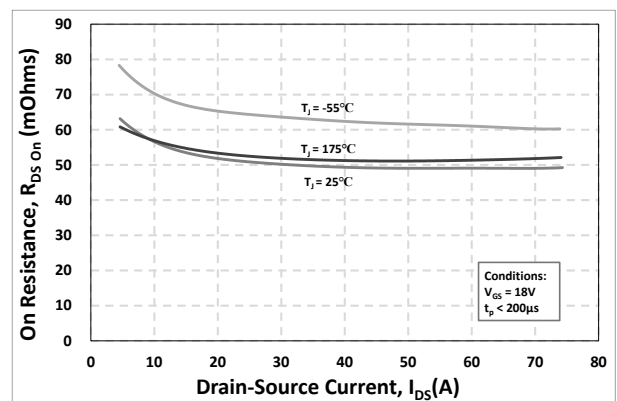


Figure 6. On-Resistance vs. Drain Current Various Temperatures



# P3M06060T3 SiC MOS N-Channel Enhancement Mode

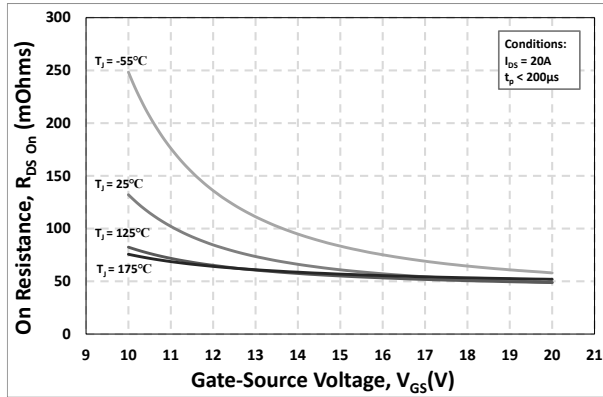


Figure 7. On-Resistance vs. Gate-Source Voltage

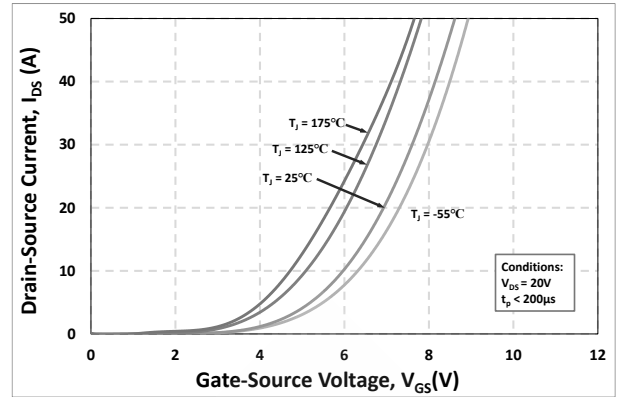


Figure 8. Transfer Characteristic for Various Junction Temperatures

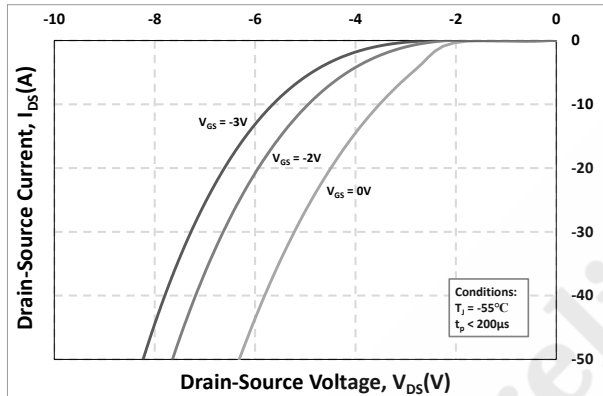


Figure 9. Body Diode Characteristic at -55°C

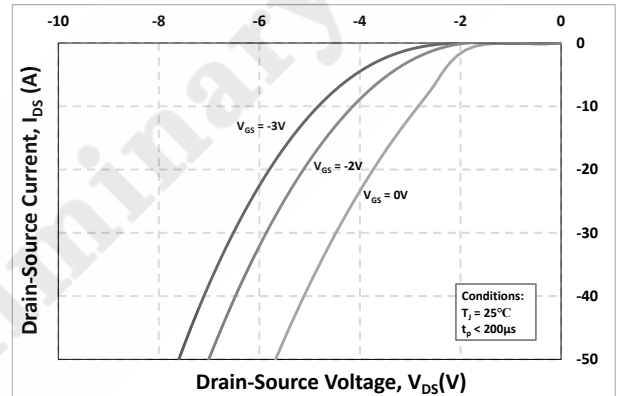


Figure 10. Body Diode Characteristic at 25°C

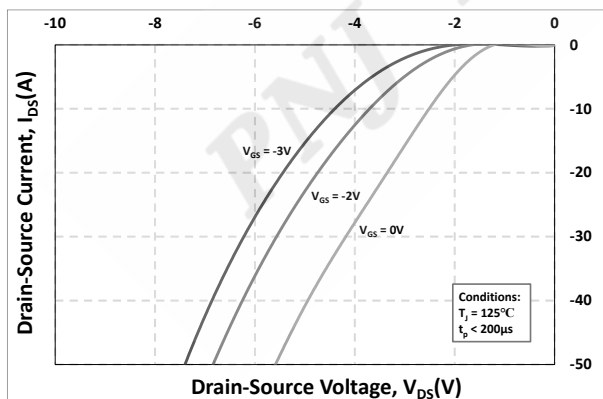


Figure 11. Body Diode Characteristic at 125°C

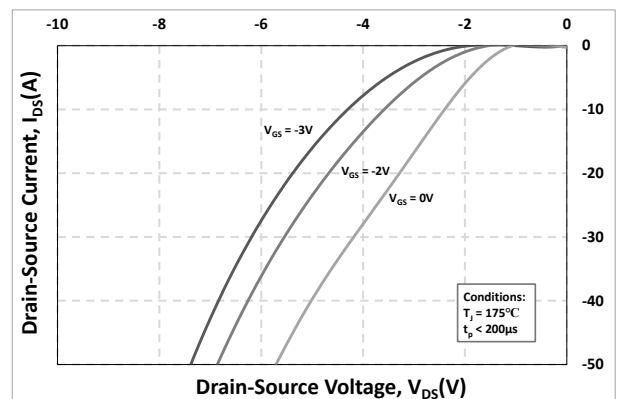


Figure 12. Body Diode Characteristic at 175°C



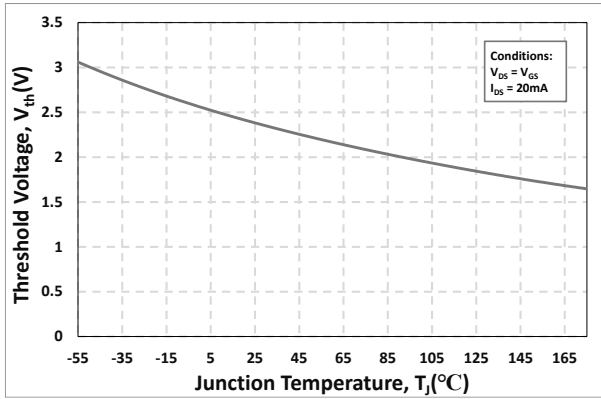


Figure 13. Threshold Voltage vs. Temperature

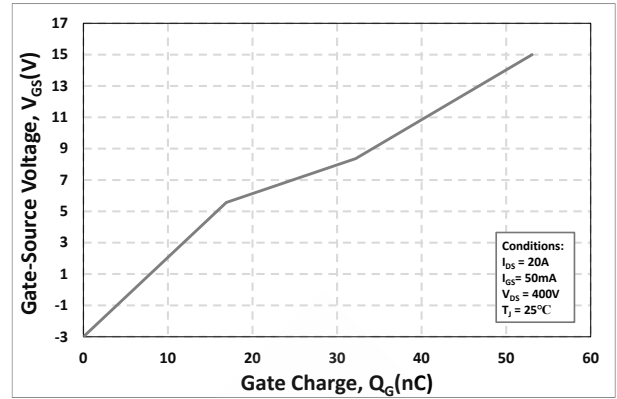


Figure 14. Gate Charge Characteristics

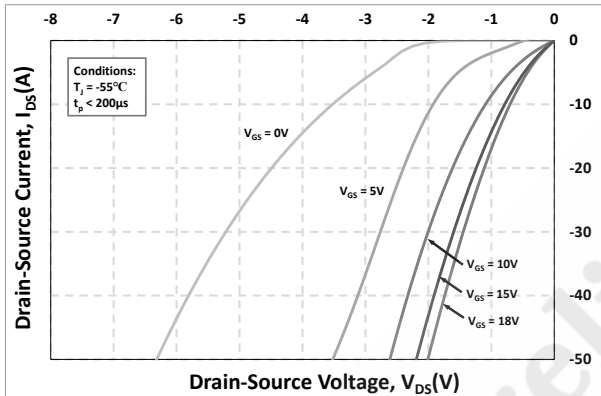


Figure 15. 3rd Quadrant Characteristic at -55°C

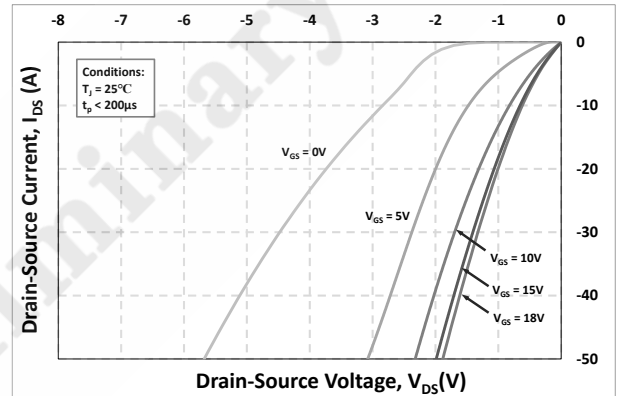


Figure 16. 3rd Quadrant Characteristic at 25°C

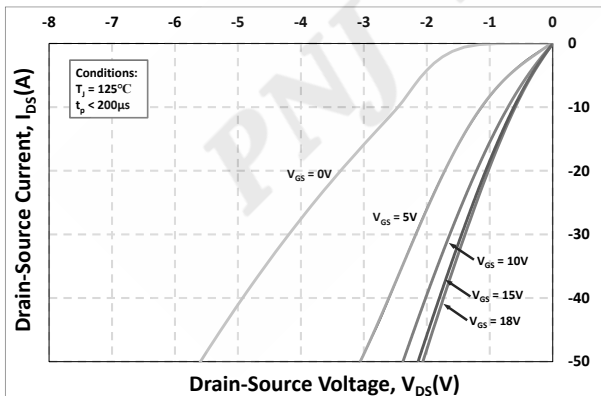


Figure 17. 3rd Quadrant Characteristic at 125°C

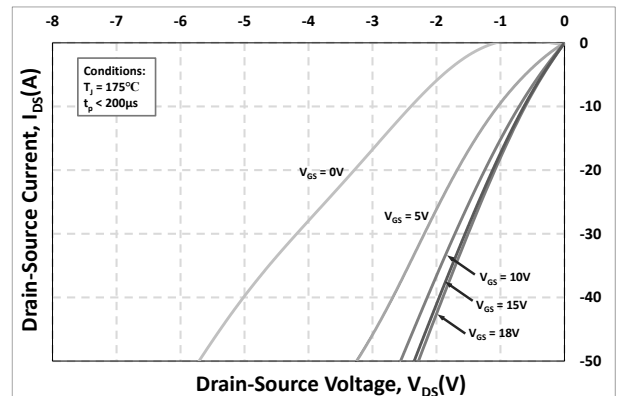


Figure 18. 3rd Quadrant Characteristic at 175°C

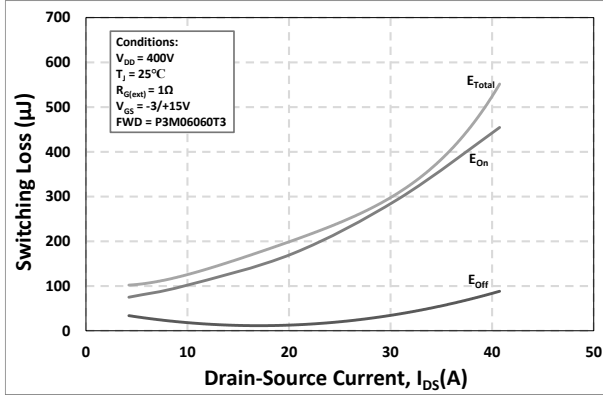


Figure 19. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 400V$ )

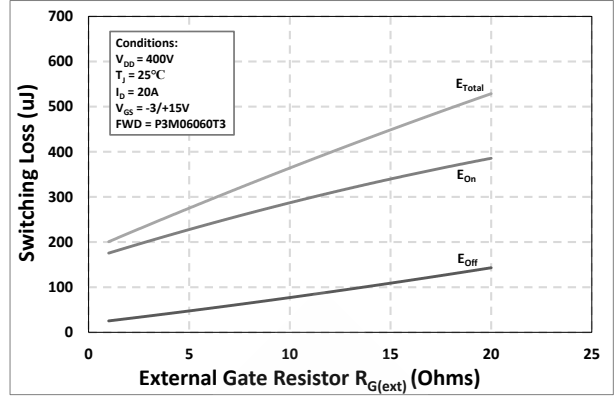


Figure 20. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

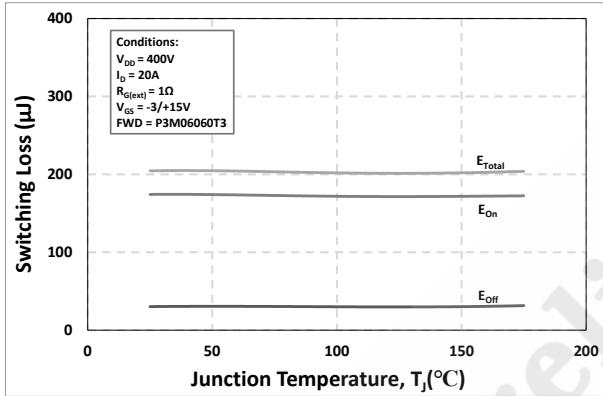


Figure 21. Clamped Inductive Switching Energy vs. Temperature

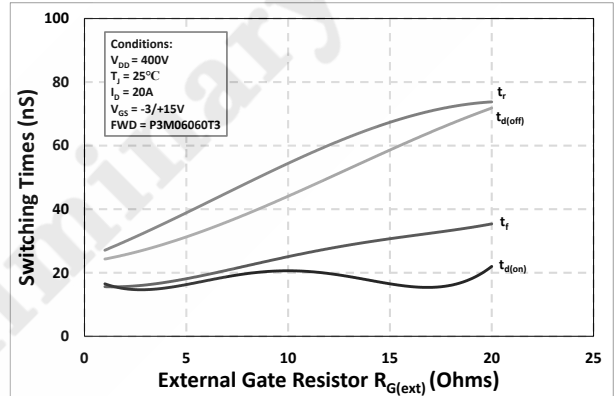


Figure 22. Switching Times vs.  $R_{G(ext)}$

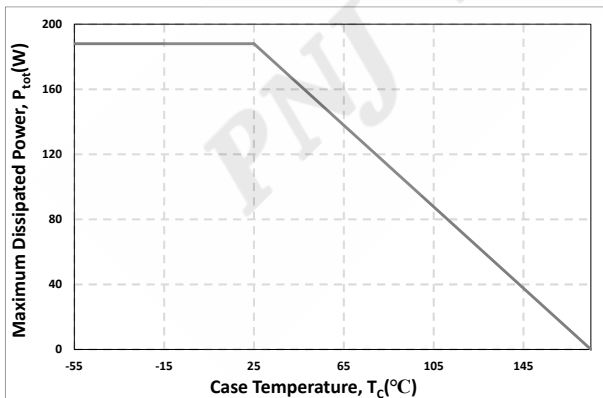


Figure 23. Maximum Power Dissipation Derating vs. Case Temperature

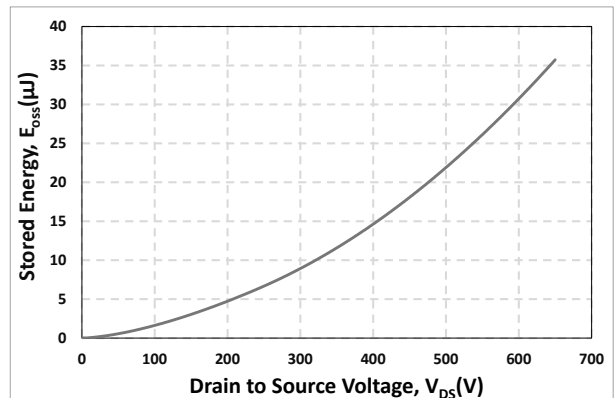


Figure 24. Output Capacitor Stored Energy

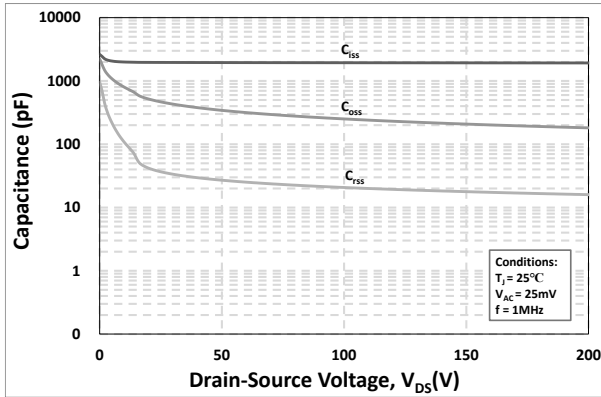


Figure 25. Capacitances vs. Drain-Source Voltage (0 - 200V)

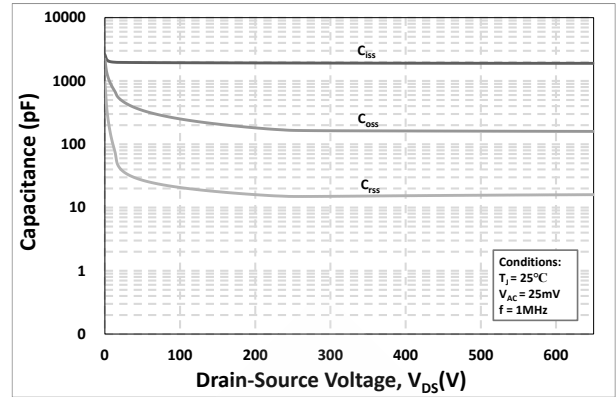


Figure 26. Capacitances vs. Drain-Source Voltage (0 - 650V)

## 6. Definitions

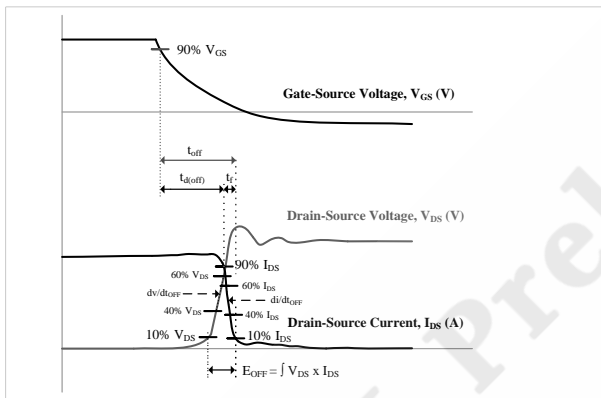


Figure 27. Turn-off Transient Definitions

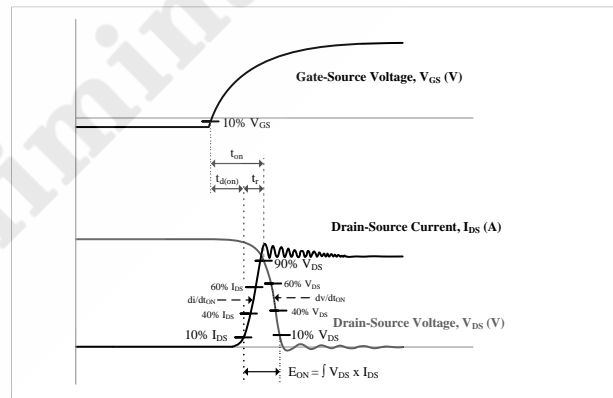


Figure 28. Turn-on Transient Definitions

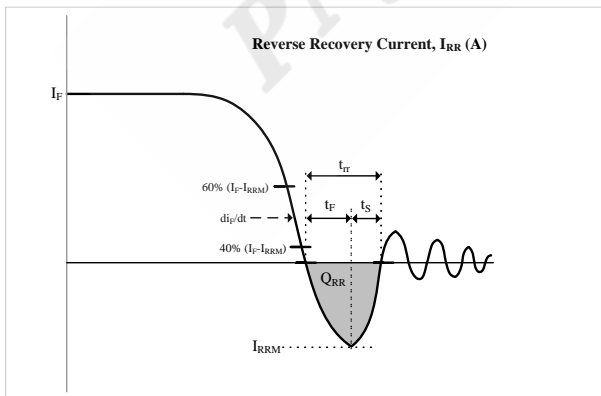


Figure 29. Reverse Recovery Definitions

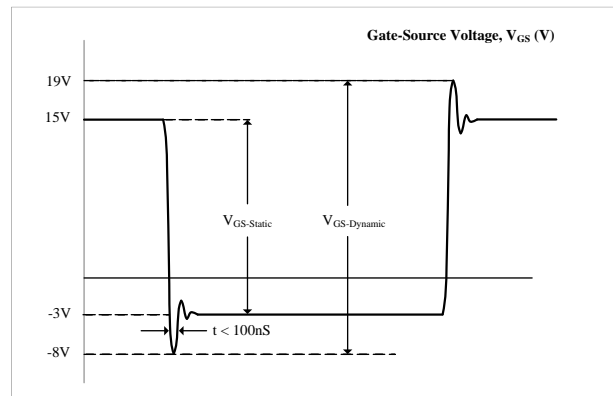
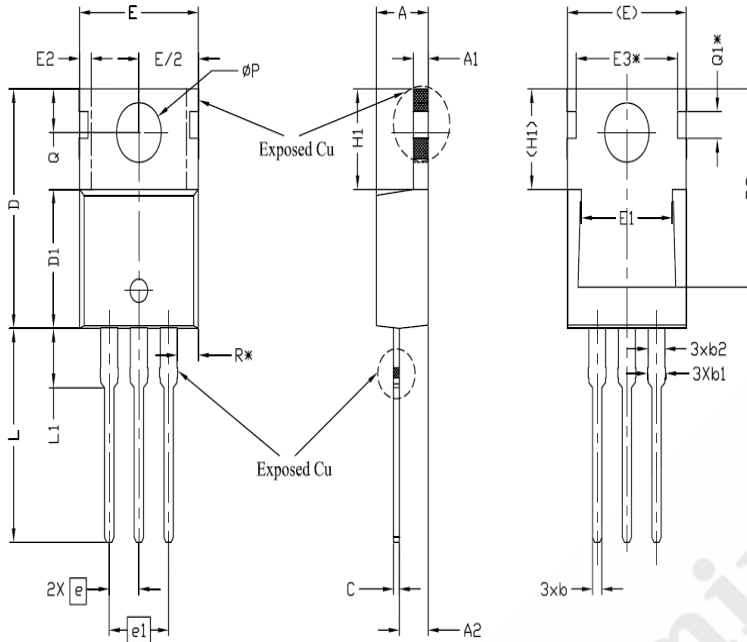


Figure 30. Vgs Transient Definitions

## 7. Package Outlines



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1.20	1.55	1.75	
b2	1.20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8.82	8.92	9.02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6.86	7.77	8.89	5
E2	-	-	0.76	6
E3*	8.70REF.			
e	2.54BSC			
e1	5.08BSC			
H1	6.30	6.45	6.60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
$\phi P$	3.75	3.84	3.93	
Q	2.60	2.80	3.00	
Q1*	1.73REF.			
R*	1.82REF.			

Drawing and Dimensions

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